REMARKS

Present Status of the Application

In the Office Action dated February 26, 2003, the Examiner rejected claims 1, 3 and 4 under 35 U.S.C. 102(b) as being anticipated by Yu, USPN 5,869,873. Furthermore, claims 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Ker et al., USPN 5,754,380. Claims 1-4 remain pending in the present application with no changes. New claims 13 and 14 have been added. For at least the following reasons, Applicants respectfully submit that claims 1-4, 13 and 14 are in proper condition for allowance. Reconsideration is respectfully requested.

Response to Rejections under 35 U. S. C. 102(b)

The Office Action rejected claims 1 and 3-4 under 35 U. S. C. 102(b) as being anticipated by Yu et al., USPN 5,869,873. Applicants respectfully disagree and traverse the rejections as set forth below.

In response to argument filed January 07, 2003, the Office Action stated that "Yu teaches that EPROM 4 triggers the SCR circuit (col. 5, line 48)." Applicants agree with the statement, but would like to point out that EPROM 4 of the cited reference is not an anti-latch up circuit. EPROM 4 of Yu triggers on the SCR circuit when ESD occurs, however, the anti-latch-up circuit of the present invention as defined in claim 1 prevents the SCR circuit when no ESD occurs. The RC circuit in Yu's Fig. 6 cannot be the anti-latch up circuit either because EPROM provides no signal output to the SCR circuit so it cannot prevent the latch up of the SCR circuit. In the

claimed invention, the anti-latch up circuit, as such as the RC circuit (which is one embodiment of the anti-latch up circuit), provides a voltage signal (a high voltage in this embodiment) to the third terminal of the SCR circuit to prevent it from latch up during normal operation because the third terminal can serve as the guard ring.

In the claimed invention, the sixth terminal of the anti-latch up circuit is coupled to the third terminal of SCR circuit. *The Office Action in page 2, line 11 to page 3, line 2, states that this is similar to the line connection between the RC elements and the third connection terminal of the SCR circuit is done via transistor 4 (EPROM in Yu's Fig. 6).* Applicants respectfully disagree, and would like to point out that in Yu's invention, EPROM is used to trigger SCR circuit due to its low breakdown voltage (col.4, line 60 – col.5, line10). It cannot provide any voltage to the third terminal of SCR circuit since it is in a normal off state (its control gate is ground via resistor R). The only voltage applied to the ESD circuit in Yu is from the ESD current during an electrostatic discharge. Therefore, the EPROM 4 of the cited reference does not perform the same function as the anti-latch-up circuit of the present invention. Col. 5, lines 45-56, of Yu clearly states that the EPROM 4 of Yu activates the SCR circuit when ESD occurs, whereas the anti-latch-up circuit of the present invention prevents the SCR circuit from activating when no ESD occurs. From the above discussion, it is clear that, Yu does not teach an anti-latch-up circuit which sends an anti-latch-up signal to the SCR circuit.

Claim 3 requires that the node between R & C of RC circuit (one embodiment of the anti-latch up circuit) be coupled to the second N+ doped region of SCR circuit. The Office Action stated that in Yu's invention, RC circuit is also coupled to the second N+ region via transistor 55

(EPROM) as shown in Yu's Fig. 5& 6. Applicants respectfully disagree and would like to point out that in fact, the transistor 55 (EPROM) of Yu is in normally off state during the normal operation. Therefore, it couples nothing from RC circuit to the second N+ doped region of SCR circuit.

With regard to claim 4, according to Yu's description (col.5, line 24-40), RC circuit in Yu's Fig.6 is used to program "EPROM" to raise its threshold voltage from 0.7V to 1.1~2V during ESD event. That's why the output node of RC circuit is coupled to the control gate of EPROM, instead of the node 33 in Yu's Fig.6. In the claimed invention, however, RC circuit (one embodiment of the anti-latch up circuit) is used to avoid the latch up of SCR circuit by providing a voltage signal to the third terminal of SCR circuit during normal operation. Thus, its output terminal (sixth connection terminal in Claim1) is coupled to Node A instead of the control gate of EPROM. In fact, EPROM is needed to lower the trigger of SCR in Yu's invention but not in case of the claimed invention.

For at least the foregoing reasons, claims 1, and 3-4 patently define over Yu. Reconsideration of the rejection to the claims is respectfully requested.

Response to Rejections under 35 U. S. C. 103

The Office Action rejected claim 2 under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Ker et al. (US-5,754,380, hereinafter Ker).

Applicants respectfully disagree and would like to particularly point out that even though Ker is relied upon for showing a first diode and a second diode, still Ker cannot cure the specific

deficiencies of Yu. Accordingly, Applicants respectfully submit that claim 2 patently define over Yu and Ker, and reconsideration and withdrawal of these rejections is respectfully requested.

New Claims

New claims 13 and 14 depend from claim 1 and further define the present invention. They are believed patentable for at least the reasons discussed above.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-4, 13 and 14 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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Date: 6/6/2003

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